PCN 14_0066

ADG5233/ADG5234 Data Sheet Changes

Rev. B to Rev. C

This document highlights the performance differences between the Rev.B and Rev.C Transfer for the ADG5233 and ADG5234 Analog Multiplexers.

For full product information and changes to Typical Performance Characteristics plots please refer to the ADG5233/34 Rev.C data sheet.

1. HBM ESD

HBM ESD	Rev B	Rev C
I/O Port to Supplies	4 kV	8 kV
I/O Port to I/O Port	1 kV	2 kV
All other pins	4 kV	8 kV

2. Datasheet specification changes from Rev. B to Rev. C

Tables 1 to 4 outline a datasheet specification comparison of Rev. B to Rev. C material. The changed specifications are highlighted in red font.

SPECIFICATION CHANGES FROM Rev. B to Rev. C

Table 1. $V_{DD} = +15\ V \pm 10\%$, $V_{SS} = -15\ V \pm 10\%$, GND = 0 V, unless otherwise noted.

Parameter	Rev. B 25°C	Rev. B −40°C to +85°C	Rev. B −40°C to +125°C	Rev. C 25°C	Rev. C −40°C to +85°C	Rev. C −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH								
Analog Signal Range			V_{DD} to V_{SS}			V_{DD} to V_{SS}	V	
	160			160			Ω typ	$V_S = \pm 10\ V$, $I_S = -1\ mA$
On Resistance, R_{ON}	200	250	280	200	250	280	Ω max	$V_{DD} = +13.5\ V$, $V_{SS} = -13.5\ V$
On-Resistance Match Between Channels, ΔR_{ON}	3.5			3.5			Ω typ	$V_S = \pm 10\ V$, $I_S = -1\ mA$
	8	9	10	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	38			38			Ω typ	$V_S = \pm 10\ V$, $I_S = -1\ mA$
	50	65	70	50	65	70	Ω max	
LEAKAGE CURRENTS								$V_{DD} = +16.5\ V$, $V_{SS} = -16.5\ V$
Source Off Leakage, I_S (Off)	±0.02			±0.02			nA typ	$V_S = \pm 10\ V$, $V_D = \pm 10\ V$
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			±0.02			nA typ	$V_S = \pm 10\ V$, $V_D = \pm 10\ V$
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			±0.08			nA typ	$\pm V_S = V_D = \pm 10\ V$
	±0.2	±0.3	±0.9	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2			2	V min	
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			0.002			µA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			3			pF typ	
Dynamic Characteristics[1]								
Transition Time, $t_{TRANSITION}$	170			125			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ pF$
	210	250	280	160	190	215	ns max	$V_S = 10\ V$
t_{ON} (EN)	175			145			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ pF$
	215	255	290	175	210	240	ns max	$V_S = 10\ V$
t_{OFF} (EN)	80			125			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ pF$
	100	115	125	155	170	180	ns max	$V_S = 10\ V$
Break-Before-Make Time Delay, t_D	60			45			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ pF$
			30			25	ns min	$V_{S1} = V_{S2} = 10\ V$
Charge Injection, Q_{INJ}	−0.6			0.4			pC typ	$V_S = 0\ V$, $R_S = 0\ \Omega$, $C_L = 1\ nF$
Off Isolation	−75			−76			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ pF$, $f = 1\ MHz$
Channel-to-Channel Crosstalk	−80			−87			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ pF$, $f = 1\ MHz$
−3 dB Bandwidth	205			355			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\ pF$
Insertion Loss	−6.3			−6.4			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ pF$, $f = 1\ MHz$
C_S (Off)	4.5			2.8			pF typ	$V_S = 0\ V$, $f = 1\ MHz$
C_D (Off)	10			9			pF typ	$V_S = 0\ V$, $f = 1\ MHz$
C_D (On), C_S (On)	15			13			pF typ	$V_S = 0\ V$, $f = 1\ MHz$
POWER REQUIREMENTS								$V_{DD} = +16.5\ V$, $V_{SS} = -16.5\ V$
I_{DD}	45			45			µA typ	Digital inputs = 0 V or V_{DD}
	55		70	55		70	µA max	
I_{SS}	0.001			0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1			1	µA max	
V_{DD}/V_{SS}			±9/±22			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design, not subject to production test.

Table 2. V_{DD} = +20V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Parameter	Rev.B 25°C	Rev.B −40°C to +85°C	Rev.B −40°C to +125°C	Rev. C 25°C	Rev. C −40°C to +85°C	Rev. C −40°C to +125°C	Unit	Test Conditions/ Comments
ANALOG SWITCH								
Analog Signal Range			V_{DD} to V_{SS}			V_{DD} to V_{SS}	V	V_S = ±15 V, I_S = −1 mA
On Resistance, R_{ON}	140			140			Ω typ	
	160	200	230	160	200	230	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			3.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	8	9	10	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	33			33			Ω typ	V_S = ±15 V, I_S = −1 mA
	45	55	60	45	55	60	Ω max	
LEAKAGE CURRENTS								V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.02			±0.02			nA typ	V_S = ±15 V, V_D = ±15 V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			±0.02			nA typ	V_S = ±15 V, V_D = ±15 V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			±0.08			nA typ	± V_S = V_D = ±15 V
	±0.2	±0.3	±0.9	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2			2	V min	
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			3			pF typ	
Dynamic Characteristics[1]								
Transition Time, $t_{TRANSITION}$	170			125			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	235	260	155	180	200	ns max	V_S = 10 V
t_{ON} (EN)	165			145			ns typ	R_L = 300 Ω, C_L = 35 pF
	200	240	265	170	200	220	ns max	V_S = 10 V
t_{OFF} (EN)	80			125			ns typ	R_L = 300 Ω, C_L = 35 pF
	95	105	115	155	160	170	ns max	V_S = 10 V
Break-Before-Make Time Delay, t_D	50			40			ns typ	R_L = 300 Ω, C_L = 35 pF
			30			20	ns min	V_{S1} = V_{S2} = 10 V
Charge Injection, Q_{INJ}	0			0.7			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−75			−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	−80			−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
−3 dB Bandwidth	210			370			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−5.5			−5.6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	4.5			2.8			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	10			9			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	15			13			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS								V_{DD} = +22 V, V_{SS} = -22 V
I_{DD}	50			50			µA typ	Digital inputs = 0 V or V_{DD}
	70		110	70		110	µA max	
I_{SS}	0.001			0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1			1	µA max	
V_{DD}/V_{SS}			±9/±22			±9/±22	V min/V max	GND = 0 V

1 Guaranteed by design, not subject to production test.

Table 3. V_{DD} = +12V ± 10%, V_{SS} = 0V GND = 0 V, unless otherwise noted.

Parameter	Rev.B 25°C	−40°C to +85°C	−40°C to +125°C	Rev. C 25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/ Comments
ANALOG SWITCH								
Analog Signal Range			0 V to V_{DD}			0 V to V_{DD}	V	V_S = 0 V to 10V, I_S = −1 mA
On Resistance, R_{ON}	360			360			Ω typ	
	500	610	700	500	610	700	Ω max	V_{DD} = +10.8V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	5.5			5.5			Ω typ	V_S = 0 V to 10V, I_S = −1 mA
	20	21	22	20	21	22	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	170			170			Ω typ	V_S = 0 V to 10V, I_S = −1 mA
	280	335	370	280	335	370	Ω max	
LEAKAGE CURRENTS								V_{DD} = 13.2 V, V_{SS} = 0V
Source Off Leakage, I_S (Off)	±0.02			±0.02			nA typ	V_S = 1V/10V, V_D = +10 V/1V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			±0.02			nA typ	V_S = 1V/10V, V_D = +10 V/1V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			±0.08			nA typ	$\pm V_S = V_D$ = 1 V/10V
	±0.2	±0.3	±0.9	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2			2	V min	
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			3			pF typ	
DYNAMIC CHARACTERISTICS[1]								
Transition Time, $t_{TRANSITION}$	235			165			ns typ	R_L = 300 Ω, C_L = 35 pF
	295	365	410	215	260	300	ns max	V_S = 8 V
t_{ON} (EN)	240			200			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	380	430	245	305	350	ns max	V_S = 8 V
t_{OFF} (EN)	70			130			ns typ	R_L = 300 Ω, C_L = 35 pF
	90	105	115	165	180	200	ns max	V_S = 8 V
Break-Before-Make Time Delay, t_D	125			85			ns typ	R_L = 300 Ω, C_L = 35 pF
			65			45	ns min	$V_{S1} = V_{S2}$ = 8 V
Charge Injection, Q_{INJ}	0			0			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−75			−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	−80			−87			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
−3 dB Bandwidth	172			260			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−8.7			−9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	5			3			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	11			10			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	16			14			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS								V_{DD} = 13.2 Digital inputs = 0 V or V_{DD}
I_{DD}	40			40			µA typ	
	50		65	50		65	µA max	
V_{DD}			9/40			9/40	V min/V max	GND = 0 V, Vss=0V

[1] Guaranteed by design, not subject to production test.

Table 4. $V_{DD} = +36V \pm 10\%$, $V_{SS} = 0V$ GND = 0 V, unless otherwise noted.

Parameter	Rev.B 25°C	Rev.B −40°C to +85°C	Rev.B −40°C to +125°C	Rev.C 25°C	Rev.C −40°C to +85°C	Rev.C −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH								
Analog Signal Range			0 V to V_{DD}			0 V to V_{DD}	V	
On Resistance, R_{ON}	140			140			Ω typ	$V_S = \pm 10$ V, $I_S = -1$ mA
	170	215	245	170	215	245	Ω max	$V_{DD} = +13.5$ V, $V_{SS} = -13.5$ V
On-Resistance Match Between Channels, ΔR_{ON}	3.5			3.5			Ω typ	$V_S = \pm 10$ V, $I_S = -1$ mA
	8	9	10	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT\,(ON)}$	35			35			Ω typ	$V_S = \pm 10$ V, $I_S = -1$ mA
	50	60	65	50	60	65	Ω max	
LEAKAGE CURRENTS								$V_{DD} = +16.5$ V, $V_{SS} = -16.5$ V
Source Off Leakage, I_S (Off)	±0.02			±0.02			nA typ	$V_S = \pm 10$ V, $V_D = \pm 10$ V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			±0.02			nA typ	$V_S = \pm 10$ V, $V_D = \pm 10$ V
	±0.1	±0.2	±0.4	±0.1	±0.2	±0.4	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.08			±0.08			nA typ	$\pm V_S = V_D = \pm 10$ V
	±0.2	±0.3	±0.9	±0.2	±0.3	±0.9	nA max	
DIGITAL INPUTS								
Input High Voltage, V_{INH}			2			2	V min	
Input Low Voltage, V_{INL}			0.8			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			0.002			µA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			3			pF typ	
Dynamic Characteristics[1]								
Transition Time, $t_{TRANSITION}$	205			155			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
	255	275	290	200	215	230	ns max	$V_S = 10$ V
t_{ON} (EN)	200			180			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
	240	265	290	215	235	250	ns max	$V_S = 10$ V
t_{OFF} (EN)	85			150			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
	115	115	115	190	190	190	ns max	$V_S = 10$ V
Break-Before-Make Time Delay, t_D	65			50			ns typ	$R_L = 300$ Ω, $C_L = 35$ pF
			35			25	ns min	$V_{S1} = V_{S2} = 10$ V
Charge Injection, Q_{INJ}	−0.6			0.5			pC typ	$V_S = 0$ V, $R_S = 0$ Ω, $C_L = 1$ nF
Off Isolation	−75			−76			dB typ	$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz
Channel-to-Channel Crosstalk	−80			−87			dB typ	$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz
−3 dB Bandwidth	190			275			MHz typ	$R_L = 50$ Ω, $C_L = 5$ pF
Insertion Loss	−5.9			−6.2			dB typ	$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz
C_S (Off)	4.5			2.8			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (Off)	10			9			pF typ	$V_S = 0$ V, f = 1 MHz
C_D (On), C_S (On)	15			13			pF typ	$V_S = 0$ V, f = 1 MHz
POWER REQUIREMENTS								$V_{DD} = +16.5$ V, $V_{SS} = -16.5$ V
I_{DD}	80			80			µA typ	Digital inputs = 0 V or V_{DD}
	100		130	100		130	µA max	
V_{DD}			Sep-40			Sep-40	V min/V max	GND = 0 V, Vss=0V

[1] Guaranteed by design, not subject to production test.